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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/589,109	08/10/2006	Maurits M.N. Storms	NL040142 US	6039

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EXAMINER	
COLE, BRANDON S	

ART UNIT	PAPER NUMBER
4125	

NOTIFICATION DATE	DELIVERY MODE
02/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/589,109	STORMS ET AL.	
	Examiner	Art Unit	
	BRANDON S. COLE	4125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/10/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show that transistor Q10 is a GO_2 transistor as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Mentze et al (US 7,030,654).

As to claim 1, Mentze et al figure 1 shows a voltage driver circuit for driving a device at a selected one of a plurality of voltages (High or Low) associated with respective device operations including a high voltage operation (102) and a relatively lower voltage operation (104), the driver circuit comprising an input (Input Signal), a single output (Output Signal) for connection to said device, and a plurality of voltage drivers (102 and 104) between said input and said output including at least one high voltage breakdown driver (102) and at least one relatively lower breakdown voltage driver (104) the circuit being arranged such that, during a high voltage operation, said high voltage breakdown driver-is connected to said output and there is a substantially zero voltage drop across said relatively lower breakdown voltage driver, and, during a relatively lower voltage operation, said relatively lower breakdown voltage driver provides the drive voltage for driving said device, the contribution of said high

breakdown voltage driver to said drive voltage during said relatively lower voltage operation being substantially negligible. The high voltage operation is in parallel with the low voltage operation therefore when the voltage is high the low voltage operation would technically be "off" and therefore having a zero voltage drop. Alternatively, when the voltage is low the low voltage operation provides the voltage for the circuit.

As to claim 2, Mentze et al figure 1 shows a circuit according claim 1, wherein the high voltage breakdown driver(s) comprise of an inverter consisting of high voltage breakdown transistors. Mentze et al teaches in column 2, lines 9 – 10 that the high voltage buffer stage comprises of an inverter. It is obvious to someone having ordinary skill in the art that an inverter is made of two transistors (Wikipedia – Inverter (Logic Gate)) and it would be obvious that the transistors are designated to handle a high voltage because in the reference they are attached to a high voltage.

As to claim 3, Mentze et al figure 2 shows a circuit according to claim 1, wherein the at least one relatively lower breakdown voltage driver comprises of an inverter consisting or relatively lower breakdown voltage transistors (220, 222). It is obvious to someone having ordinary skill in the art that an inverter is made of two transistors (Wikipedia – Inverter Logic Gate) and it would be obvious that the transistors are designated to handle a low voltage because in the reference they are attached to a low voltage.

As to claim 4, Mentze et al figure 1 shows a circuit according to claim1 comprising two signal paths between the input and the output, a first signal path consisting of one or more high voltage drivers (102) connected in series, and a second signal path consisting of at least one low voltage driver (104), the first and second signal paths being connected in parallel to one another.

As to claim 5, Mentze et al figure 1 shows a circuit according to claim 1comprising a means for selecting the first signal path during high voltage operation. Mentze et al teaches column 3, lines 24 – 27 that input signal resides between two logic levels (Wikipedia - Clock Signal) so that when the logic level is high the first signal path is selected.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 12 -14 are rejected under 35 U.S.C. 102(b) as being anticipated by Mentze et al (US 7,030,654), as applied to claim 1 above, and in further of Rhee (US 2001/0000949).

As to claims 12 and 13 Mentze et al fails to teach that the voltage driver circuit is part of memory device.

However, Rhee figure 5 teaches in paragraph [0011] that the driver circuit is used in an integrated circuit memory device.

Therefore it would have been obvious to one having ordinary skill in the art, at the time of the invention to use Mentze et al's voltage driver circuit in a integrated circuit memory device for the purpose of accounting for variations in loading of the memory device.

Claim 14 has similar limitations as to claim 13 above (an integrated circuit is a type of a computing system (Wikipedia – Integrated Circuits)). Therefore, the claim is rejected for the same reasons.

6. Claims 6, 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mentze et al (US 7,030,654) in view of Parkinson (US 5,889,415).

As to claim 6, Mentze et al figure 1 shows a voltage driver circuit for driving a device at a selected one of a plurality of voltages associated with respective device operations including a high voltage operation (102) and a relatively lower voltage operation (103), the driver circuit comprising an input (Input Signal), a single output (Output Signal) for connection to said device, and a plurality of voltage drivers (102 and 104) between said input and said output including at least one high voltage breakdown driver (102) and at least one relatively lower breakdown voltage driver (104), the high breakdown voltage driver comprising a voltage level shifter (208, 210, 212, and 214 of figure 2) which is connected at the input of the circuit between first and second voltage lines (VddH and Ground of figure 2), the output of said level shifter is the output of the high voltage breakdown driver, and the lower breakdown voltage driver is connected to the said first and second voltage lines (VddH and Ground of figure 2). Mentze et al teaches about the level shifter in column 4, lines 35 – 57.

Mentze et al fails to show that the output of high voltage breakdown driver is connected to the input of a relatively lower breakdown voltage.

However, Parkinson figure 1 shows at high voltage operation (114) with its output (112) being the input of a relatively lower voltage operation (116). Parkinson teaches column 1, lines 20 - 23 that the driver uses a mixed voltage supply and that Vcc2 is the lower voltage

Therefore it would have been obvious to one having ordinary skill in the art, at the time of the invention, connect Mentze et al's high voltage operation to its relatively lower voltage operation just like how Parkinson's high voltage operation is connected to

its relatively lower voltage operation, with the output of the high voltage operation being the input of a relatively lower voltage operation, for purpose of the not having the high voltage device damage the low voltage device.

As to claim 7, Mentze et al figure 2 shows that the voltage level shifter comprises of a partial level shifter (208, 210, 212, and 214). The level shifter is partial because it only connects to VddH and VddL, it cannot support the full voltage drop of VDDH to Ground.

As to claim 11, Mentze et al figure 2 shows a high voltage pull-up transistor (208) that is provided between the first voltage line (VddH)

Claims 8 -10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mentze et al (US 7,030,654) as modified by Parkinson (US 5,889,415) and applied to claim 6 above, and in further view of Chen et al (US 7,193,441).

As to claims 8 and 9, Mentze et al figure 2 further shows a relatively lower breakdown voltage (104a) comprising of an inverter (220, 222).

Mentze et al fails to show that the inverter consisting of thick gate oxide devices (GO_2 is the same thing as a thick gate oxide device (Taught in Schoellkopf et al (US 2006/0054952) paragraph [0060])).

However, Chen et al teaches in column 3, lines 27 – 36 that inverter connected to the input signal a utilize thick gate oxide layer to protect to prevent gate oxide breakdown.

Therefore, it would have been obvious for one having ordinary skill in the art, at the time of the invention, to use Chen et al's inverters in place of Mentze et al's inverters with the purpose of preventing gate oxide breakdown.

Claim 10 has similar limitations as to claim 8 above (the thick oxide layer protects the input inverter). Therefore, the claim is rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON S. COLE whose telephone number is (571)270-5075. The examiner can normally be reached on Mon - Fri 7:30-5:00 EST (Alternate Friday's Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brandon S Cole/
Examiner, Art Unit 4125

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 4125